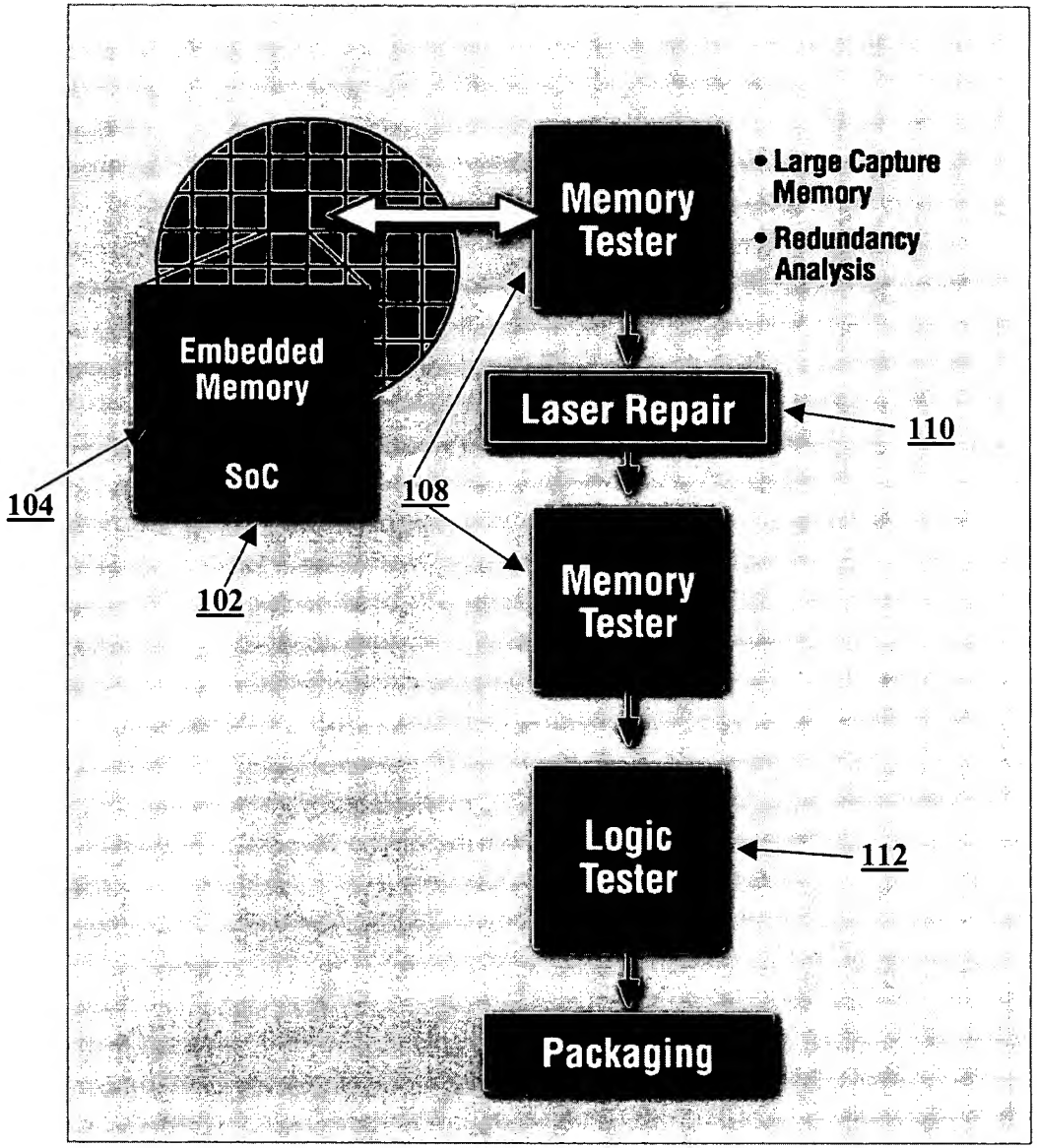


Figure 1 (Prior Art)

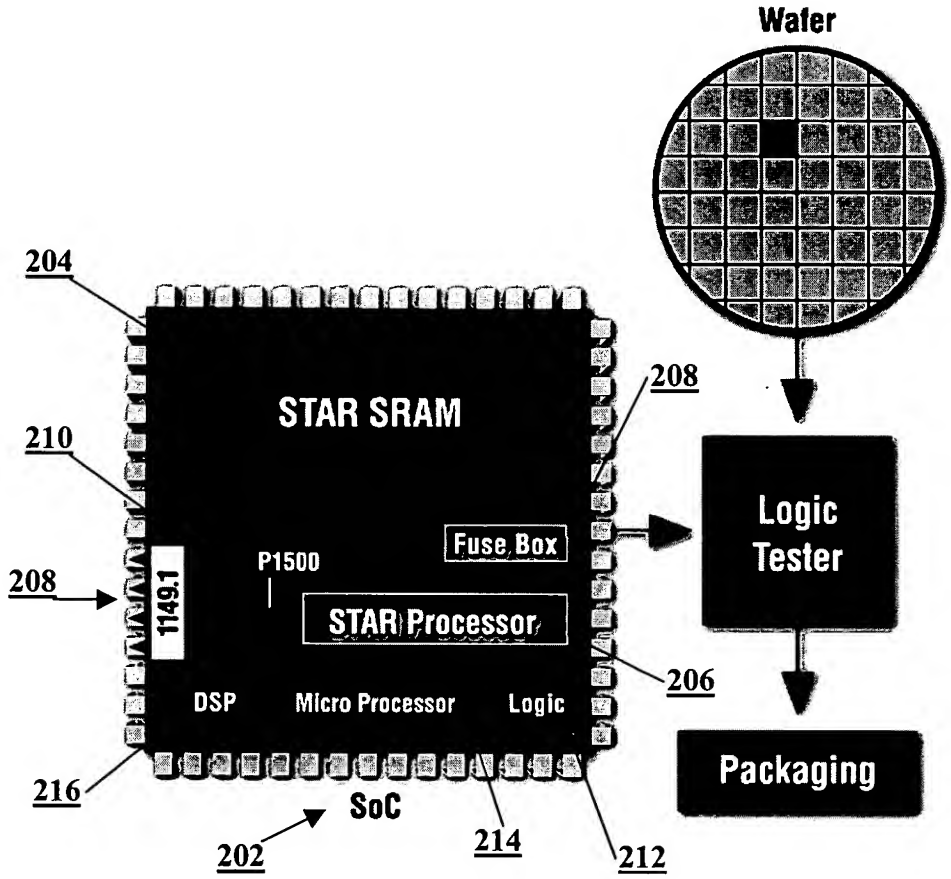

Wafer
204
STAR SRAM
208
210
Logic
Tester
Fuse Box
P1500
208
1149.1
STAR Processor
206
DSP
Micro Processor
Logic
Packaging
216
SoC
202
214
212

Figure 2a

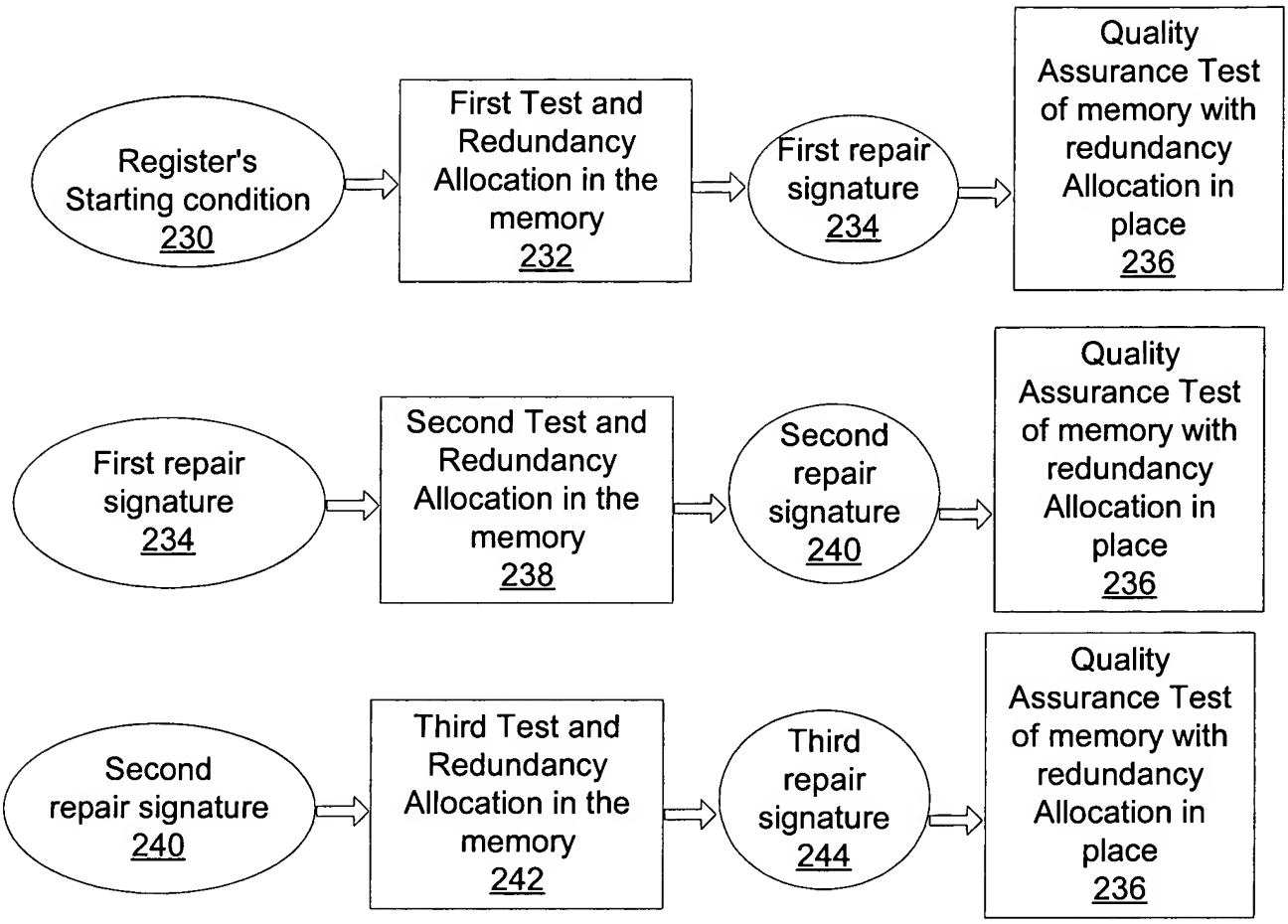

Register's Starting condition 230
First Test and Redundancy Allocation in the memory 232
First repair signature 234
Quality Assurance Test of memory with redundancy Allocation in place 236
First repair signature 234
Second Test and Redundancy Allocation in the memory 238
Second repair signature 240
Quality Assurance Test of memory with redundancy Allocation in place 236
Second repair signature 240
Third Test and Redundancy Allocation in the memory 242
Third repair signature 244
Quality Assurance Test of memory with redundancy Allocation in place 236

Figure 2b

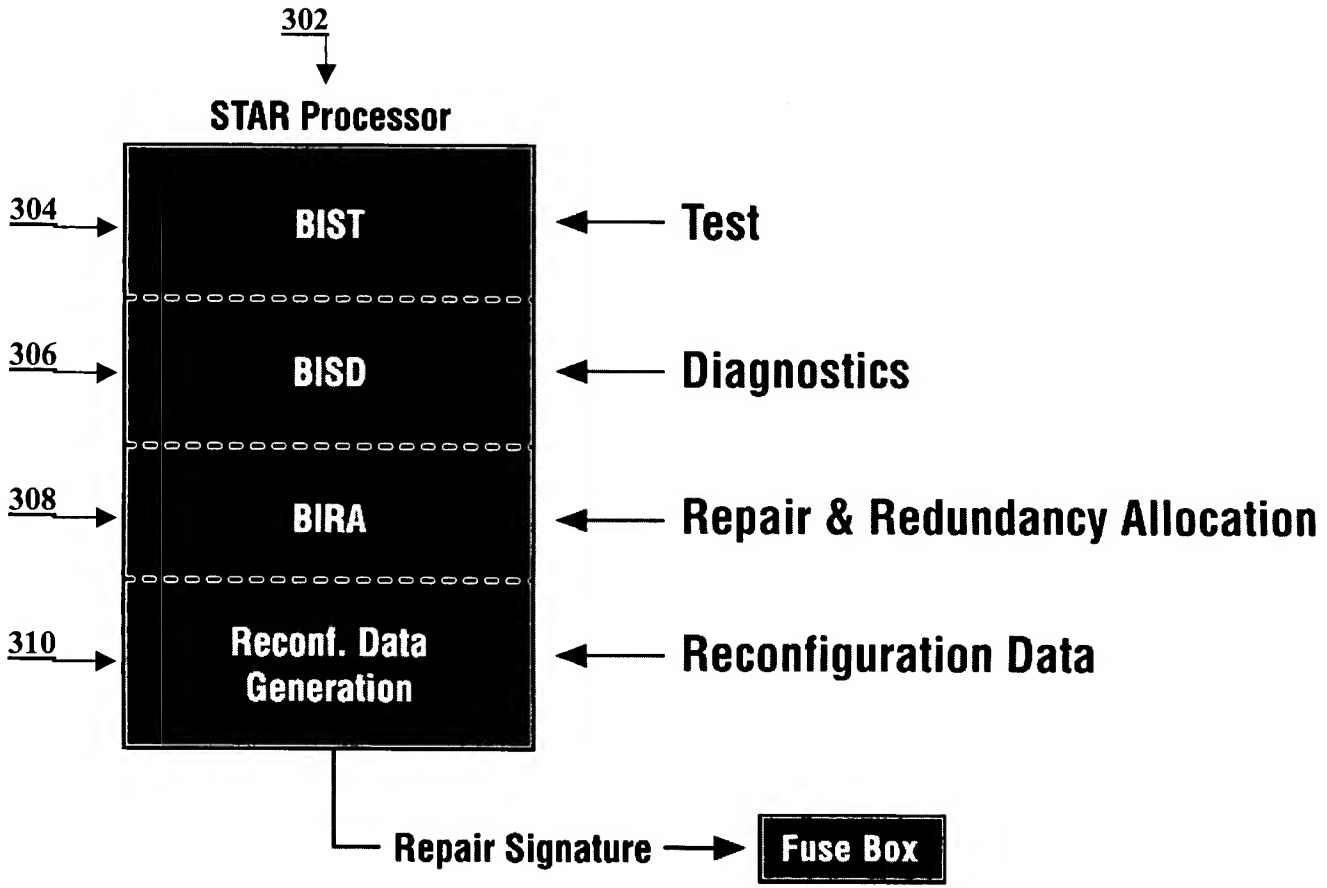

302
STAR Processor
304
BIST
Test
306
BISD
Diagnostics
308
BIRA
Repair & Redundancy Allocation
310
Reconf. Data Generation
Reconfiguration Data
Repair Signature
Fuse Box

Figure 3

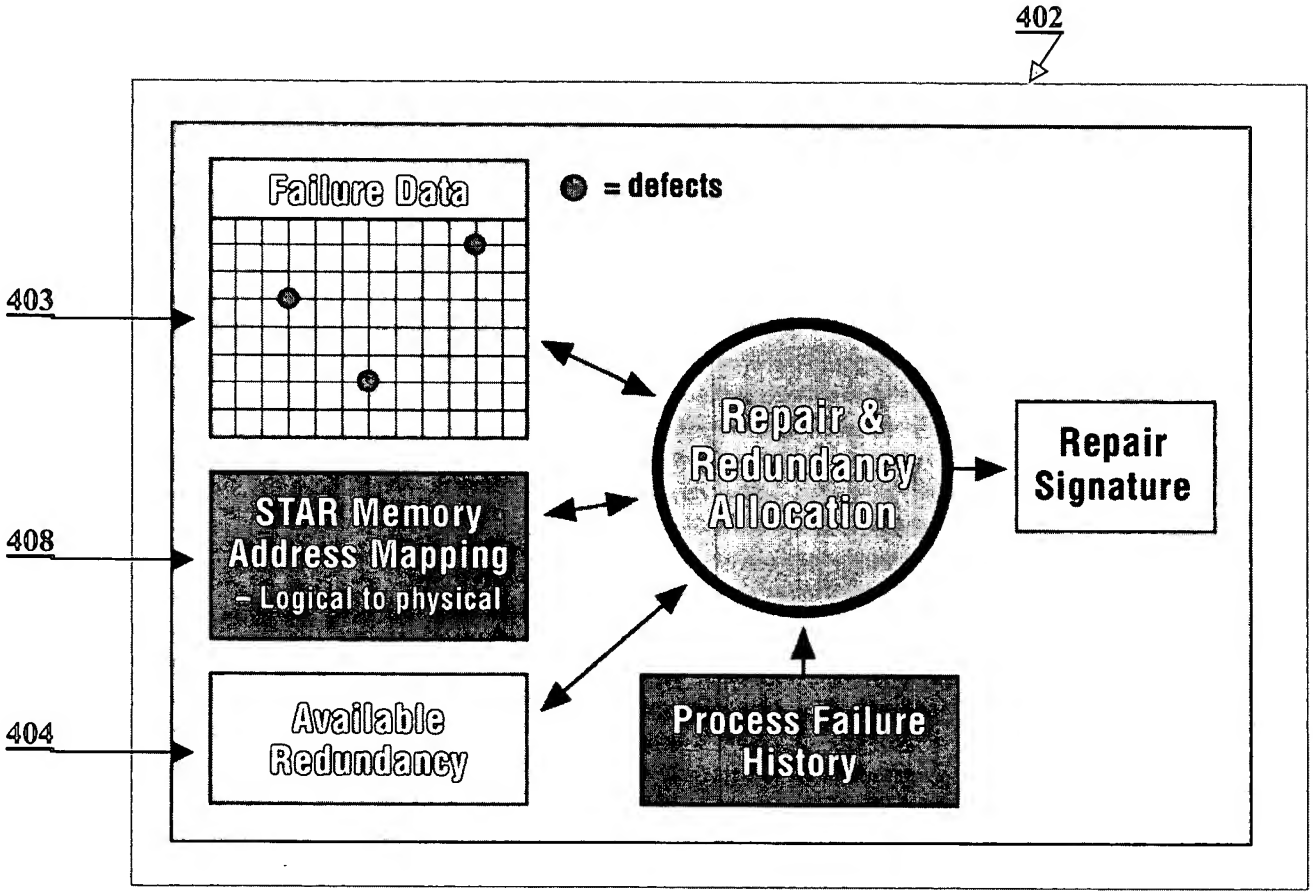

402
Failure Data
= defects
403
408
404
STAR Memory Address Mapping - Logical to physical
Available Redundancy
Repair & Redundancy Allocation
Repair Signature
Process Failure History

Figure 4a

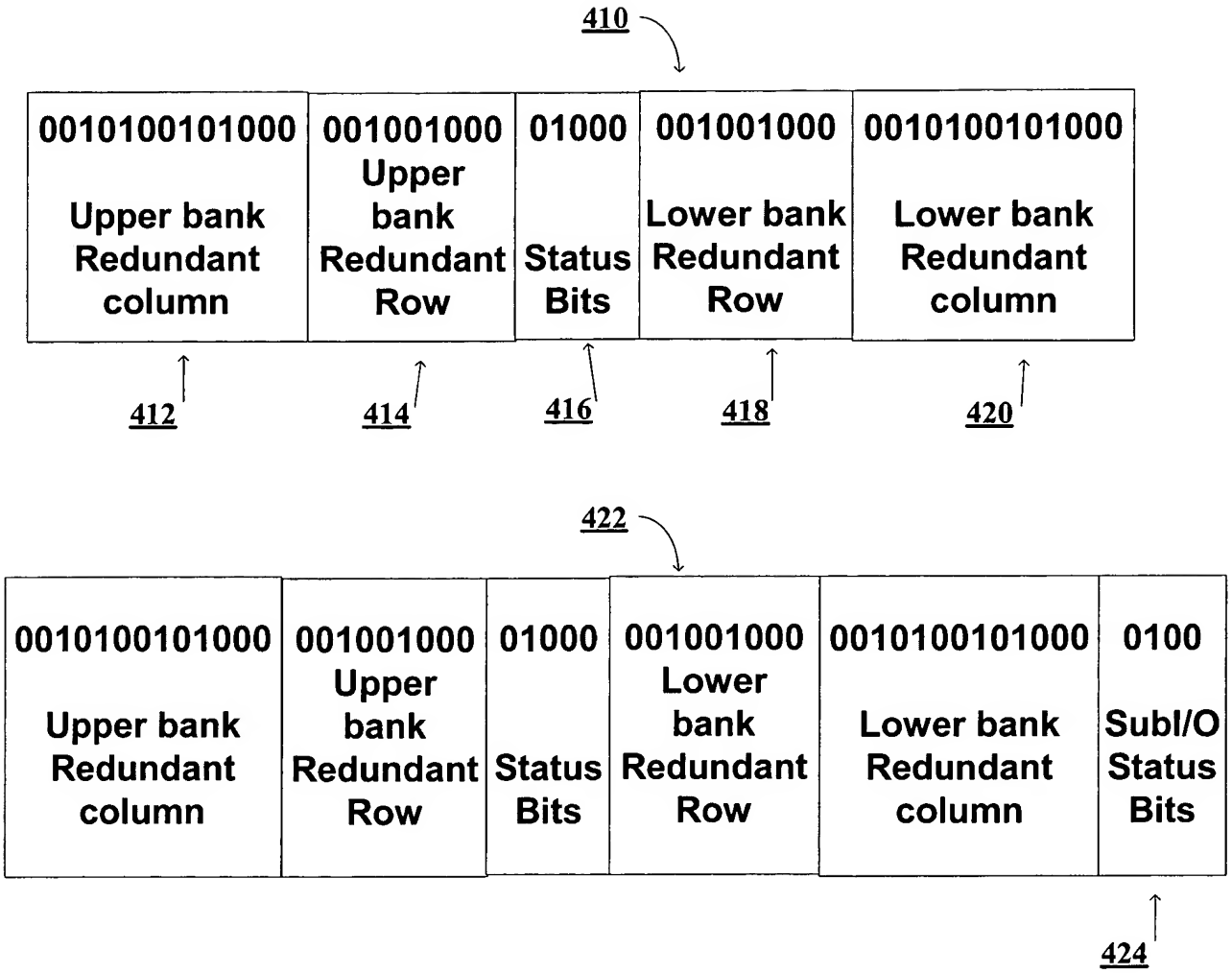

410
0010100101000
Upper bank Redundant column
001001000
Upper bank Redundant Row
01000
Status Bits
001001000
Lower bank Redundant Row
0010100101000
Lower bank Redundant column
412
414
416
418
420
422
0010100101000
Upper bank Redundant column
001001000
Upper bank Redundant Row
01000
Status Bits
001001000
Lower bank Redundant Row
0010100101000
Lower bank Redundant column
0100
SubI/O Status Bits
424

Figure 4b

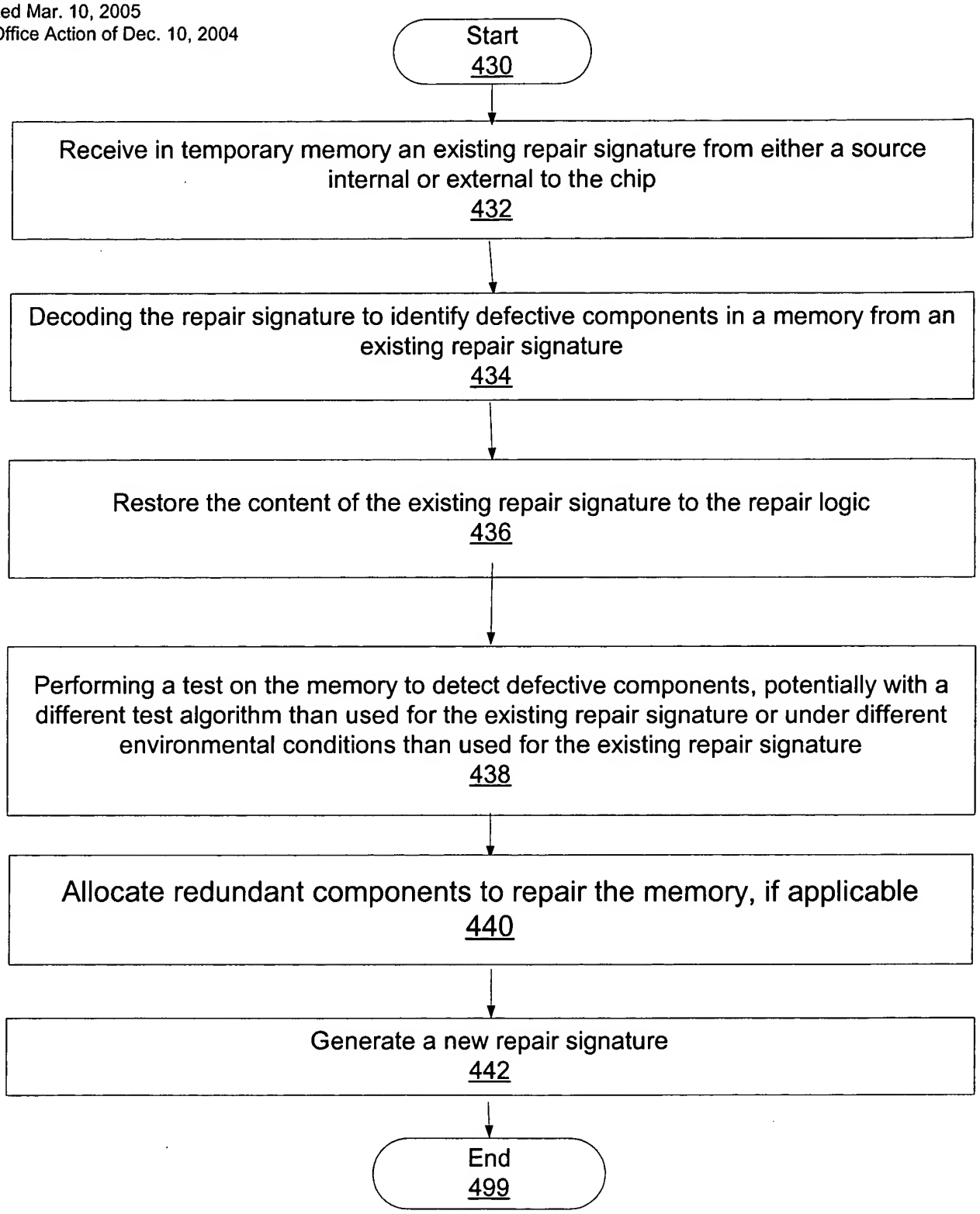

Start
430
Receive in temporary memory an existing repair signature from either a source internal or external to the chip
432
Decoding the repair signature to identify defective components in a memory from an existing repair signature
434
Restore the content of the existing repair signature to the repair logic
436
Performing a test on the memory to detect defective components, potentially with a different test algorithm than used for the existing repair signature or under different environmental conditions than used for the existing repair signature
438
Allocate redundant components to repair the memory, if applicable
440
Generate a new repair signature
442
End
499

Figure 4c

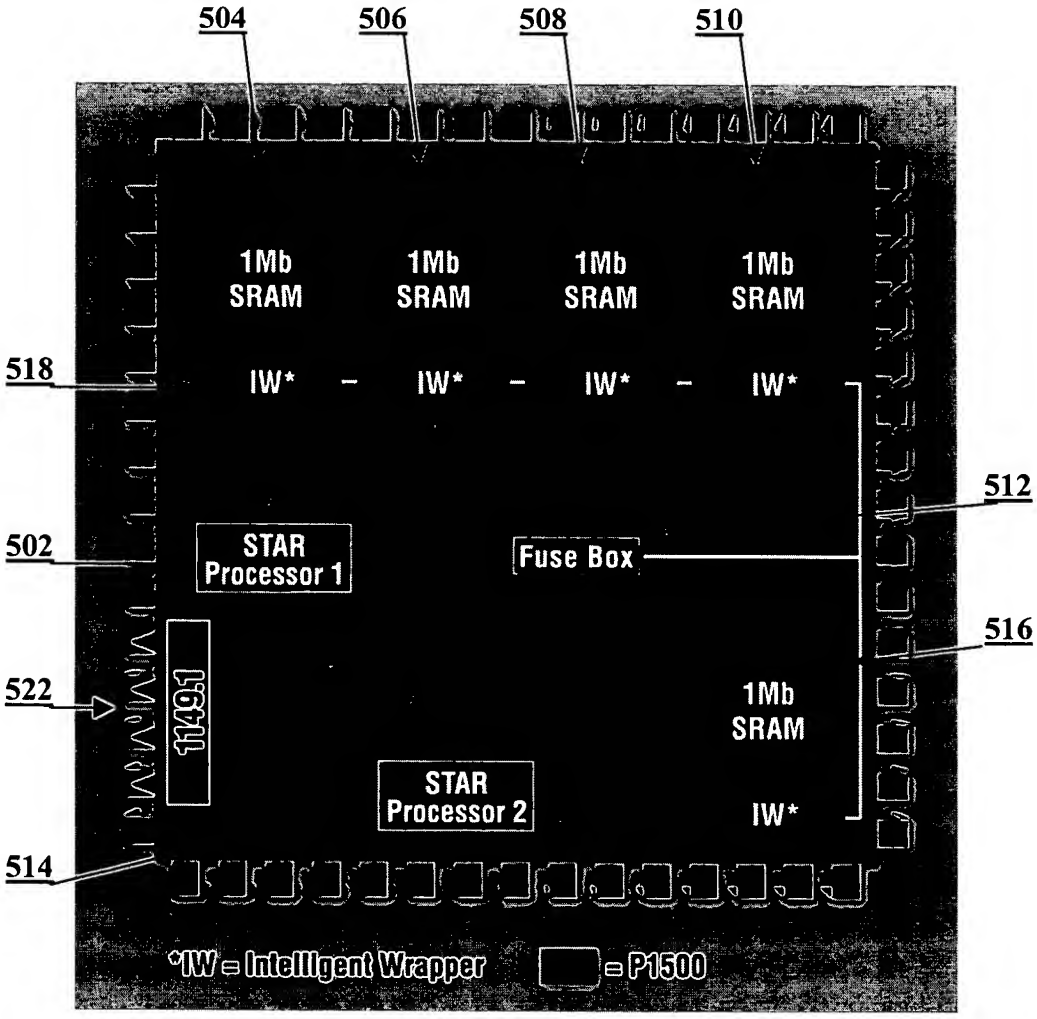

504
506
508
510
1Mb SRAM
1Mb SRAM
1Mb SRAM
1Mb SRAM
518
IW*
IW*
IW*
IW*
512
502
STAR Processor 1
Fuse Box
516
522
1149.1
1Mb SRAM
IW*
STAR Processor 2
514
*IW = Intelligent Wrapper
= P1500

Figure 5

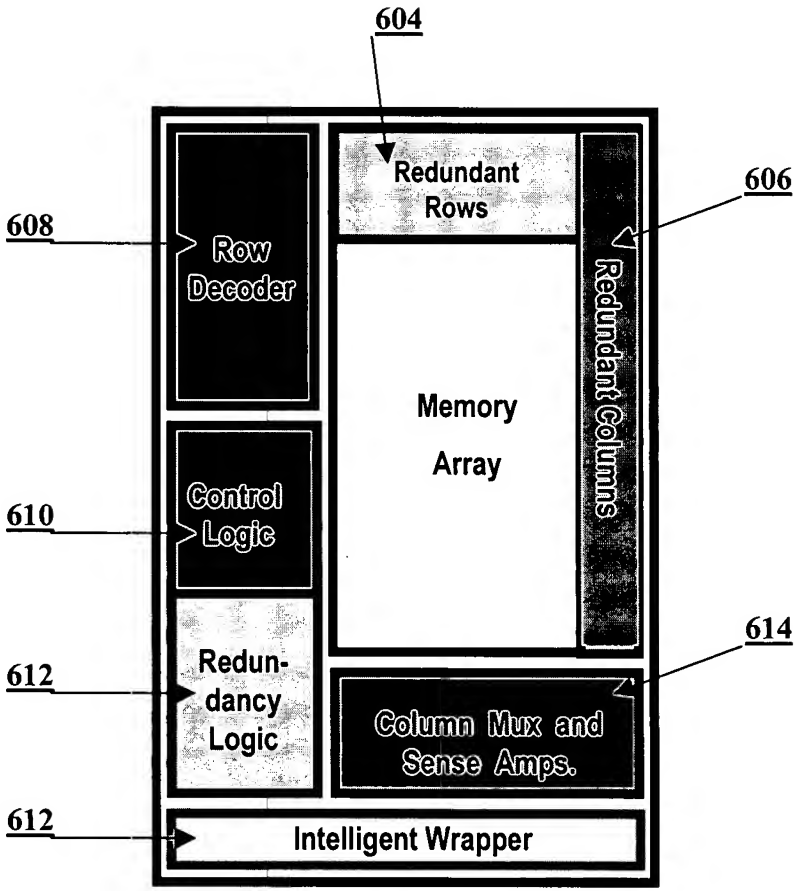

604
606
608
610
612
612
614
Redundant Rows
Row Decoder
Memory Array
Redundant Columns
Control Logic
Redun-dancy Logic
Column Mux and Sense Amps.
Intelligent Wrapper

Figure 6

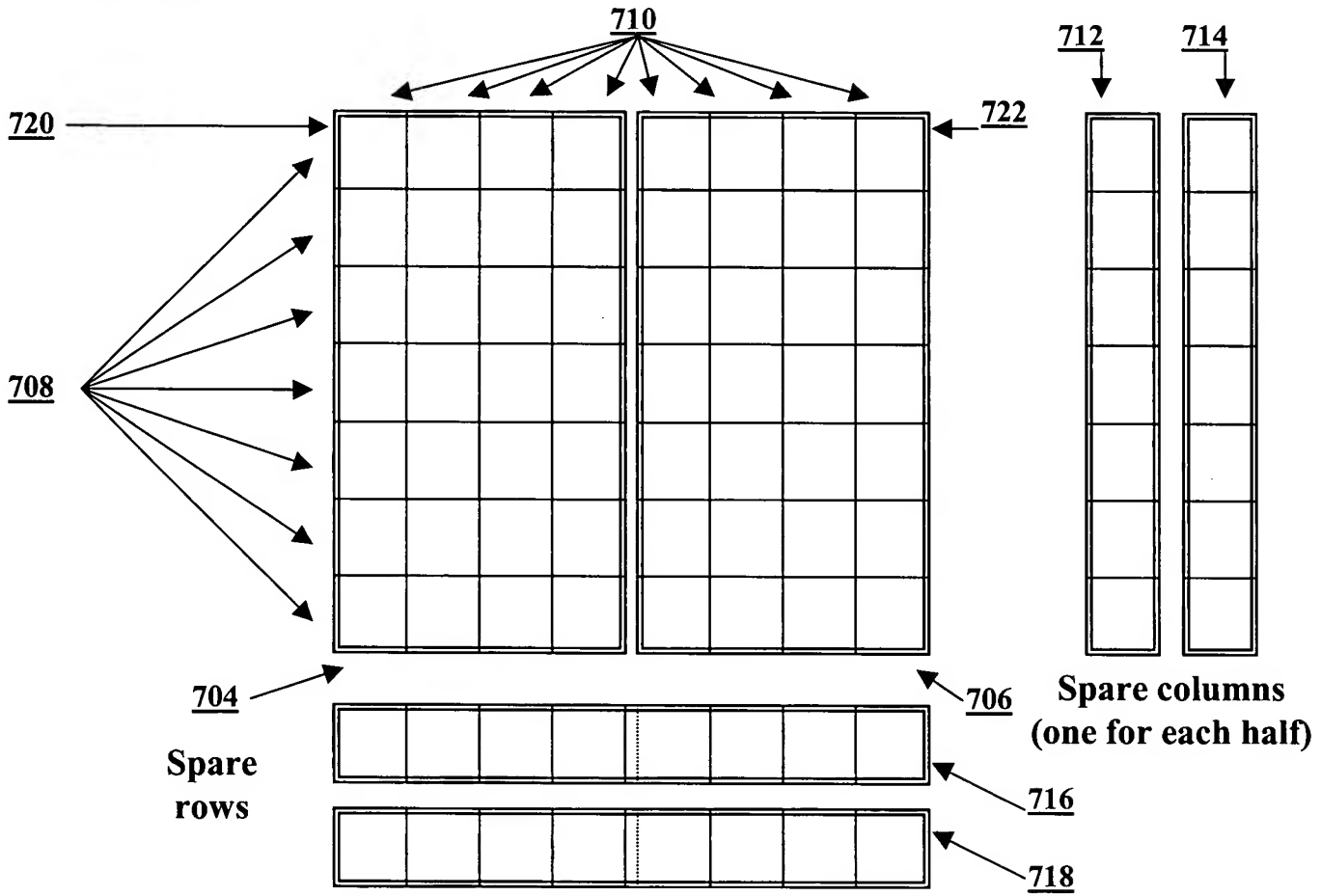

710
712
714
720
722
708
704
706
Spare columns
(one for each half)
Spare
rows
716
718

Figure 7

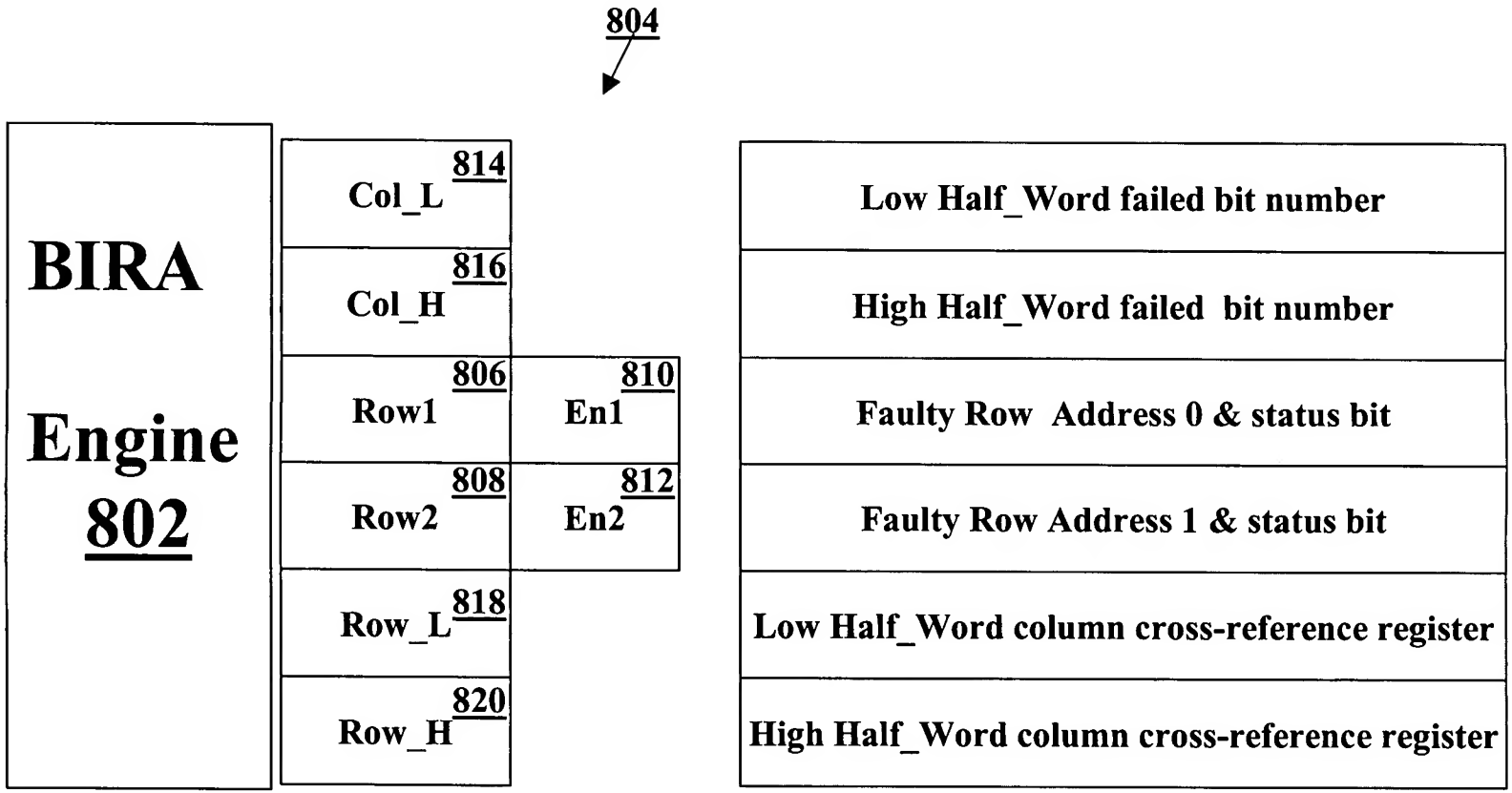

804
BIRA
Engine
802
814
Col_L
816
Col_H
806
Row1
810
En1
808
Row2
812
En2
818
Row_L
820
Row_H
Low Half_Word failed bit number
High Half_Word failed bit number
Faulty Row Address 0 & status bit
Faulty Row Address 1 & status bit
Low Half_Word column cross-reference register
High Half_Word column cross-reference register

Figure 8

Four Passes Algorithm in Order to Improve Results in the Case of Single Faults in the Row.

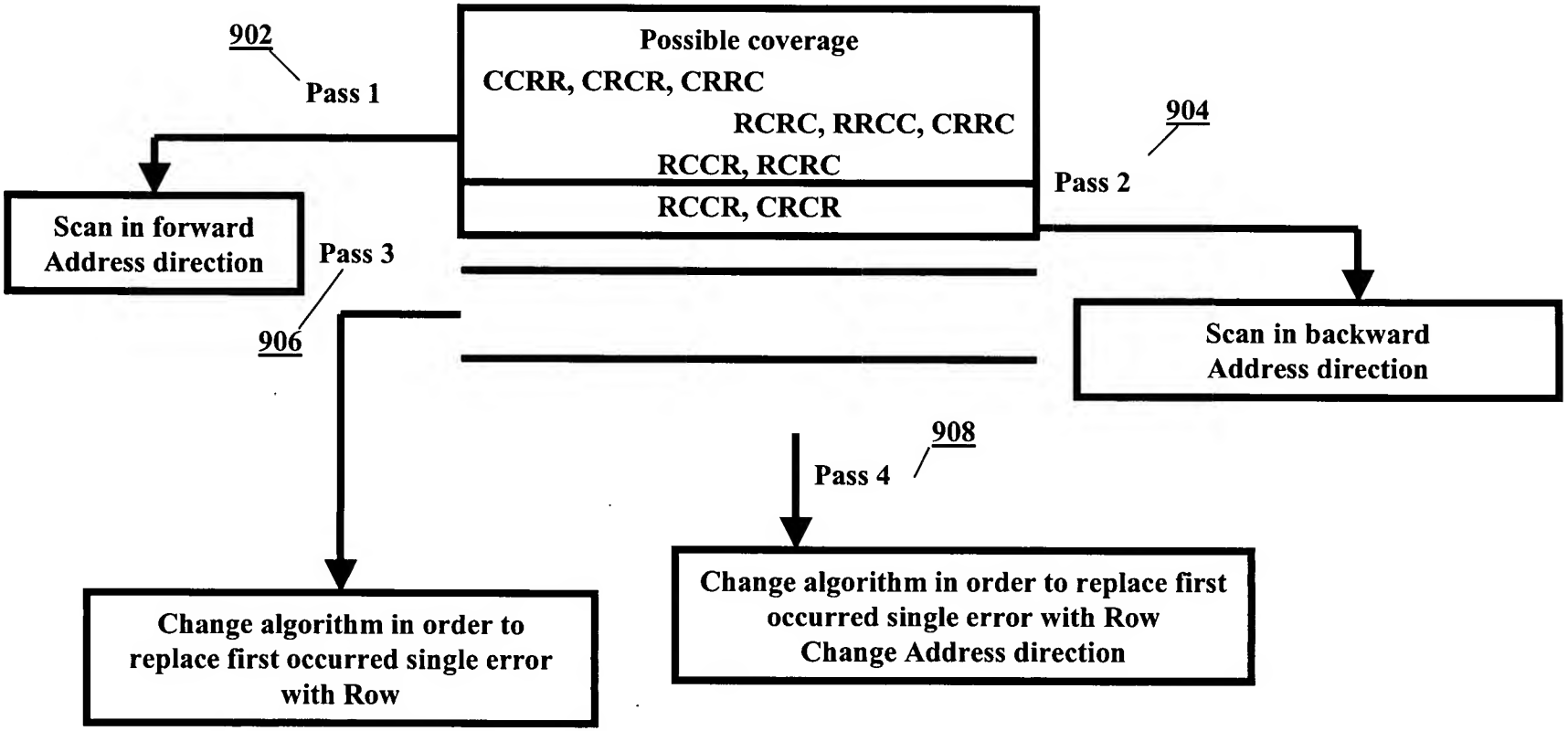
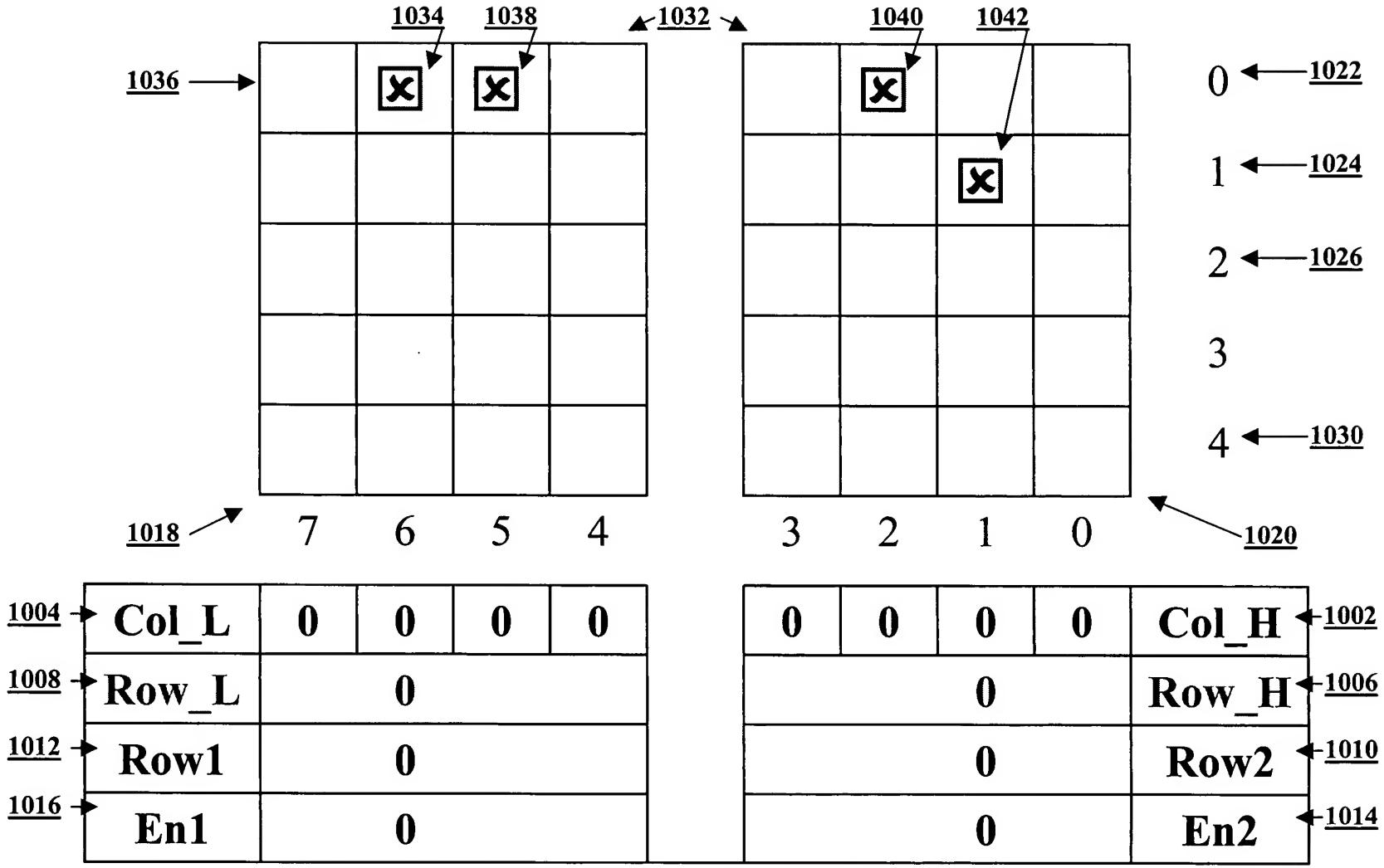
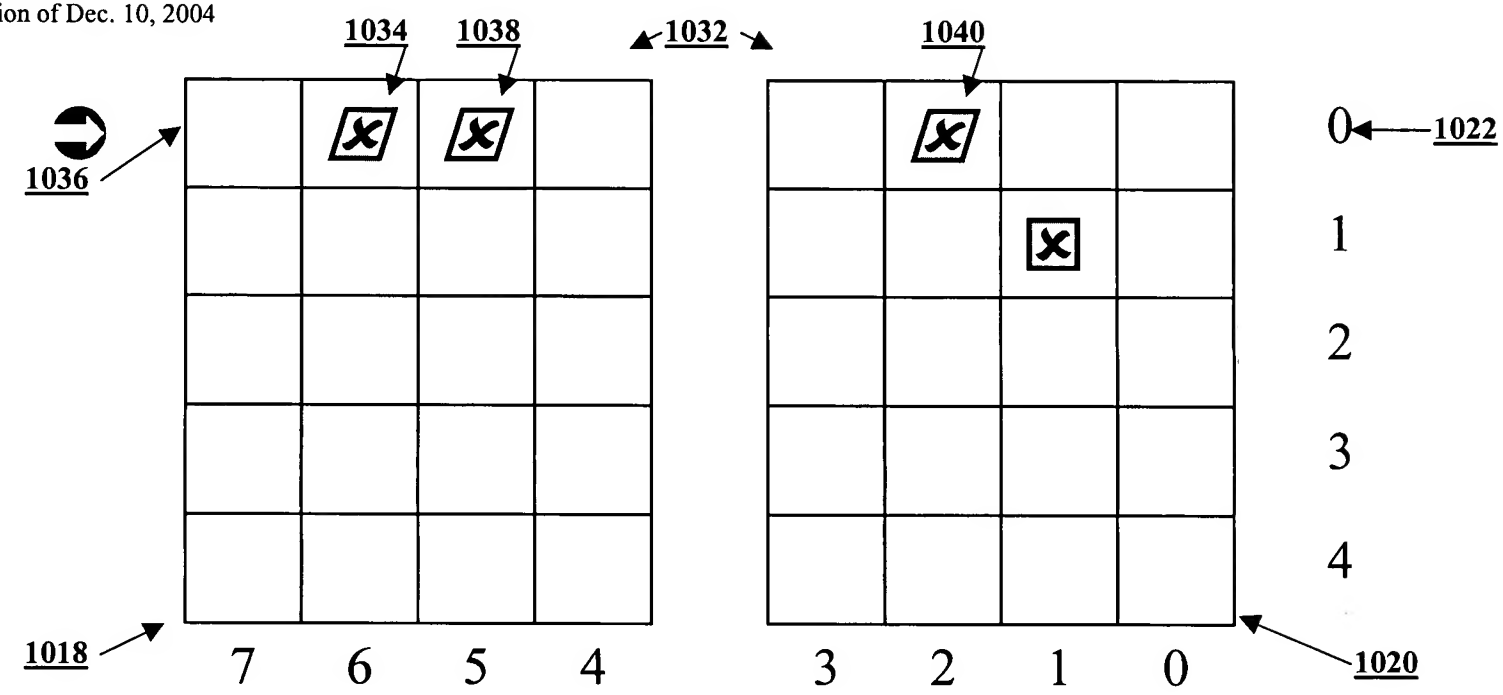


Figure 9



Start condition for BIRA registers

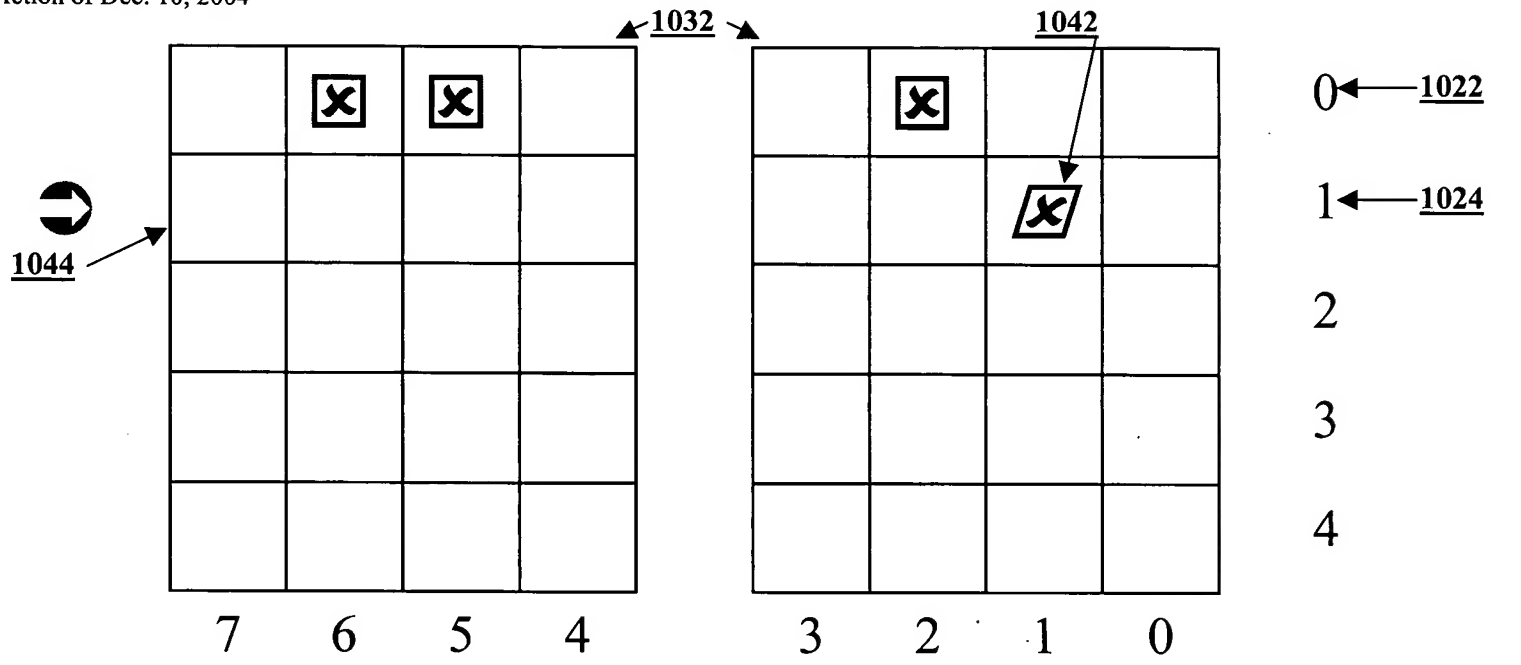
Figure 10



	Col_L	0	0	0	0	0	0	0	0	Col_H
	Row_L	0				0				Row_H
1012 →	*Row1*	*0*				0				Row2
1016 →	*En1*	*1*				0				En2

Multiple errors in Row fix with Row1

Figure 11

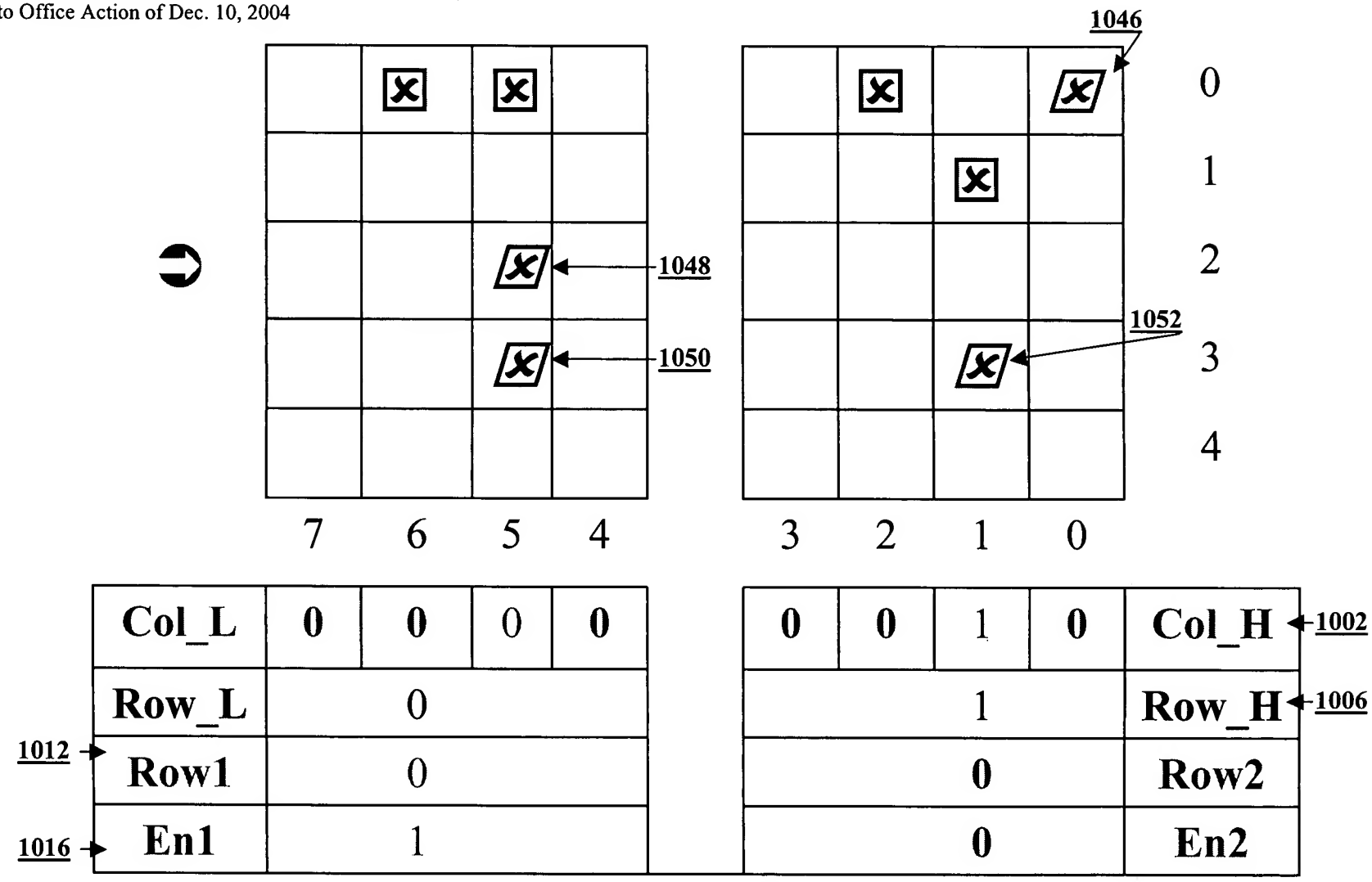


Col_L	0	0	0	0	0	0	*1*	0	Col_H
Row_L	0				*1*				Row_H
Row1	0				0				Row2
En1	1				0				En2

1002
1006

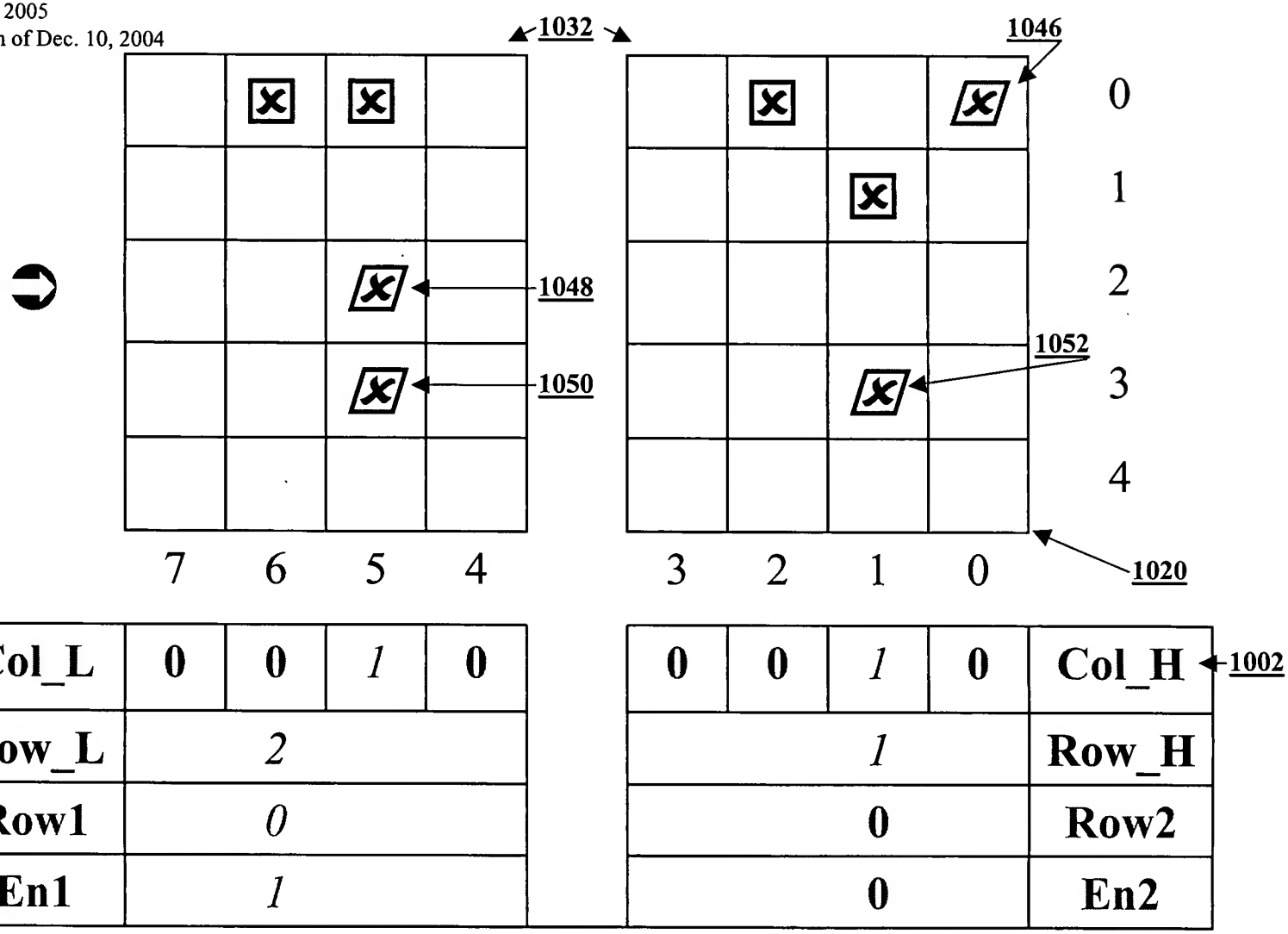
Cover single error with column, register connectivity Row_H

Figure 12



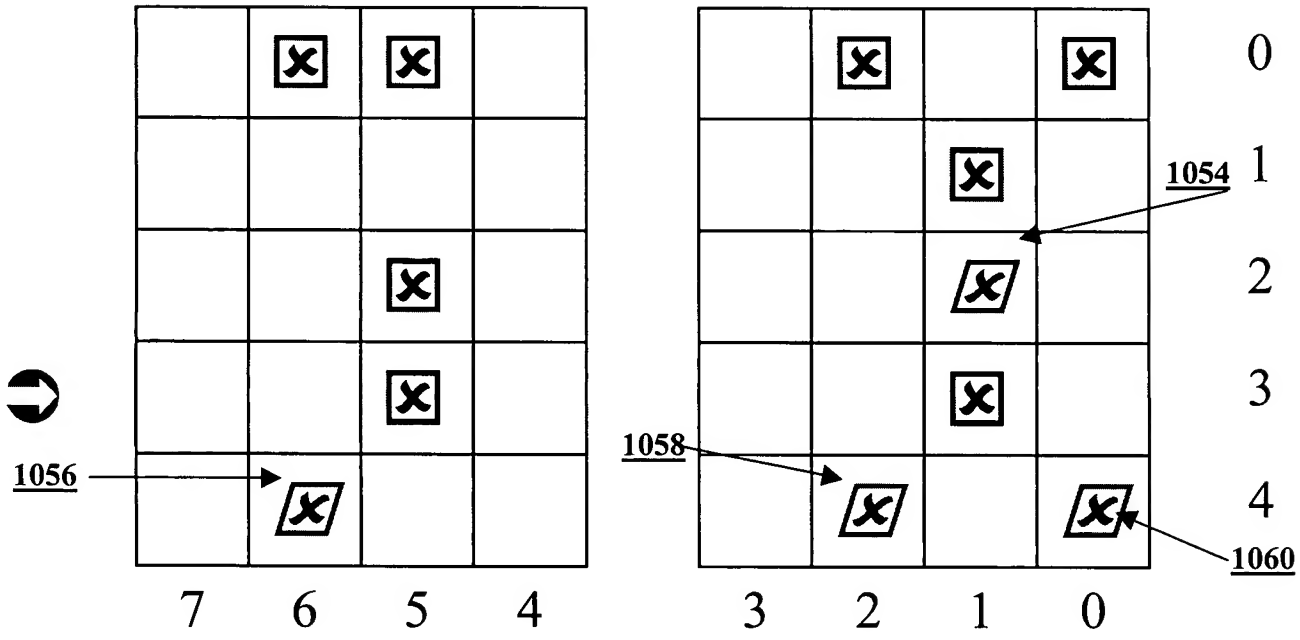
Load content of previous signature into Registers

Figure 13



Cover single error with column, register connectivity Row_L

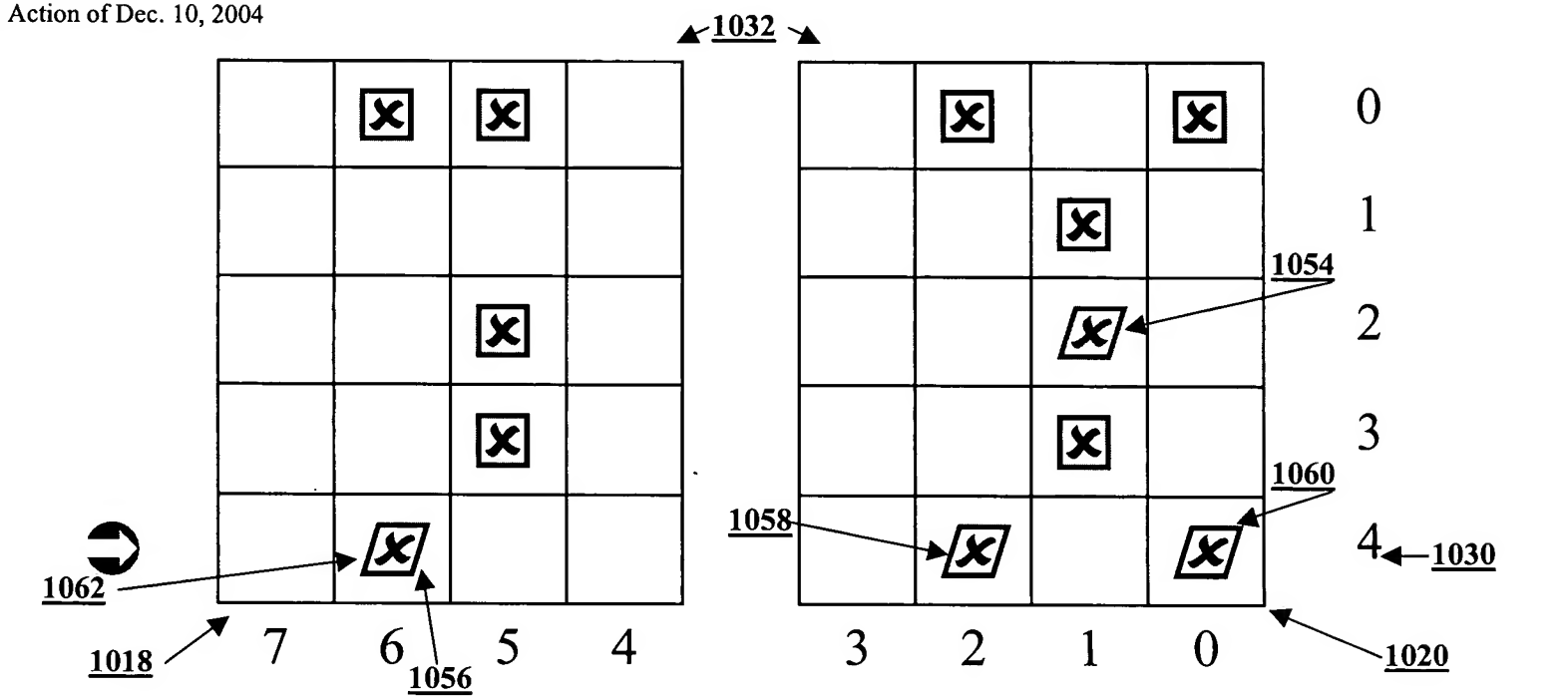
Figure 14



Col_L	0	0	1	0	0	0	1	0	Col_H
Row_L	2				1				Row_H
Row1	0				0				Row2
En1	1				1				En2

Load content of previous signature into Registers

Figure 15



Col_L	0	0	1	0	0	0	*1*	0	Col_H	1002
Row_L	2				*1*				Row_H	
Row1	0				*4*				Row2	1010
En1	1				*1*				En2	1014

Multiple errors in Row fix with Row2

Figure 16